We Claim:

1. An integrated dynamic memory, comprising:

a plurality of memory cells, the memory cells being combined to form individual independently addressable units; and

a control circuit for controlling a refresh mode for the memory cells, the memory cells having their memory cell content refreshed during the refresh mode,

the control circuit being designed such that one or more units of memory cells can be subject to the refresh mode in parallel in a refresh cycle, the control circuit setting a number of memory cell units which are to be refreshed in parallel in a refresh cycle based on a temperature reference value.

2. The integrated dynamic memory as claimed in claim 1, wherein the control circuit has a changeover mechanism such that, if a first limit temperature reference value is exceeded, a selected unit of memory cells and at least one further unit of memory cells are subject to the refresh mode in parallel in the refresh cycle.

3. The integrated dynamic memory as claimed in claim 1, wherein the memory is organized into word lines and bit lines, the memory cells being arranged at crossover points between the word lines, the memory cells bit lines and being connected to a respective word line and bit line, the memory cells in units of a whole word line subject to a refresh mode in a refresh cycle, and the control circuit sets a number of word lines which are to be refreshed in parallel in a refresh cycle based on the temperature reference value.

4. The integrated dynamic memory as claimed in claim 3, wherein the memory has a number of n word lines, the control circuit has a changeover mechanism such that, if a first limit temperature reference value is exceeded, a selected word line and a word line shifted by the number of n/2 word lines are select and are subjected to a refresh mode in parallel in a refresh cycle.

5. The integrated dynamic memory as claimed in claim 4, wherein the control circuit has a changeover mechanism such that, if a second limit temperature reference value increased by a temperature interval is exceeded, not only the selected word line and a respective word line shifted by the number of n/4, n/2, and 3n/4 word lines are subjected to a refresh mode in parallel in a refresh cycle.

6. The integrated dynamic memory as claimed in claim 5, wherein the temperature interval has been set in the control circuit to a half-value temperature which identifies a temperature interval within which the data retention time of the memory cells is halved.

7. The integrated dynamic memory as claimed in claim 1, wherein the control circuit has a counter circuit for addressing memory cell units which are to be refreshed, which receives a refresh command and a multiplexer circuit, and the multiplexer being actuated by the counter circuit for selecting the units (WL0 to WLn-1) of memory cells for a refresh mode, where the multiplexer circuit receives a control signal (R) which transmits the temperature reference value.

8. The integrated dynamic memory as claimed in claim 1, wherein the temperature reference value is generated by a temperature sensor circuit which is arranged on the memory.

9. The integrated dynamic memory as claimed in claim 1, wherein the control circuit is designed such that a plurality of units of memory cells can be subject to a refresh mode in parallel in a refresh cycle, the refresh mode being staggered over time within a refresh interval.